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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,413	04/12/2004	Peter George Hartwell	10006166-4	2570

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EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 03/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/822,413	HARTWELL, PETER GEORGE	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12,13,15,17-19,21-25 and 27-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12,15,19,21-25 and 27-31* is/are allowed.

6)☒ Claim(s) *13 and 17* is/are rejected.

7)☒ Claim(s) *18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed on 1/03/06. Currently, claims 12, 13, 15, 17-19, 21-25 and 27-31 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davey US Patent 3,663,308 in view of Ahn et al. US Patent 6,395,630.

Davey discloses the semiconductor method substantially as claimed. See figures 1a-d, and corresponding text, where Davey shows, pertaining to claim 13, a method for electrically isolating a portion of a wafer comprising: providing a first wafer **11** (figure 1a; col. 2, lines 51-55); forming a first conductor **12** at least partially through the first wafer (figures 1a and 1b; col. 1, lines 23-25; col. 2, lines 51-53, ***Note***: the Examiner takes the position that Davey teaches that the devices are interconnected into a circuit by metallization, In addition, conventionally via structures include an insulating layer surrounding theses structures, as a result it is inherent that the semiconductor devices will include conductors (via structures)); disposing first dielectric material **12** between the first conductor and material of the first wafer (figures 1a and 1b; col. 1, lines 23-25; col. 2, lines 51-53 , ***Note***: the Examiner takes the position that Davey teaches that the devices are interconnected into a circuit by metallization, In addition, conventionally via

structures include an insulating layer surrounding theses structures, as a result it is inherent that the semiconductor devices will include conductors (via structures)); and at least partially surrounding the first conductor and the first dielectric material with second dielectric material **14/16**, the second dielectric material being spaced from the first dielectric material such that a first portion of the material of the first wafer is arranged between the first dielectric material and the second dielectric material and a second portion of the material of the first wafer is arranged outside an outer periphery of the second dielectric material (figure 1d; col. 2, lines 67-75; col. 3, lines 1-3), wherein the first wafer has a first side and an opposing second side, and the first conductor extends through the first wafer from the first side to the second side, and further comprising: forming a second conductor **13** through the first wafer from the first side to the second side, the second side conductor being arranged between the first dielectric material and the second dielectric material **15** (figure 1d; col. 2, lines 67-75; col. 3, lines 1-3).

However, Davey fails to show, pertaining to claim 13, providing a second wafer; forming a first conductor at least partially through the second wafer; disposing first dielectric material between the first conductor and material of the second wafer; and at least partially surrounding the first conductor and the first dielectric material of the second wafer with second dielectric material, the second dielectric material of the second wafer being spaced from the first dielectric material of the second wafer such that a first portion of the material of the second wafer is arranged between the first dielectric material of the second wafer is arranged outside an outer periphery of the second dielectric material of the second wafer; and arranging the second wafer and the first wafer such that the first conductor of the first wafer and the first conductor of the second wafer electrically communicate with each other. In addition, Davey fails to show

pertaining to claim 17, wherein the second wafer has a first side and an opposing second side, and the first conductor of the second wafer extends through the second wafer from the first side to the second side, and further comprising: forming a second conductor through the second wafer from the first side to the second side, the second conductor of the second wafer being arranged between the first dielectric material and the second dielectric material of the second wafer.

Ahn teaches, in figures 1-10 and corresponding text, a similar method of integrated circuit fabrication that includes the formation of similar via structures where the semiconductor wafers are stacked (col. 3, lines 20-22 and 30-67; col. 5, lines 1-13).

It would have been obvious to one of ordinary skill in the art to substitute the following steps of: providing a second wafer; forming a first conductor at least partially through the second wafer; disposing first dielectric material between the first conductor and material of the second wafer; and at least partially surrounding the first conductor and the first dielectric material of the second wafer with second dielectric material, the second dielectric material of the second wafer being spaced from the first dielectric material of the second wafer such that a first portion of the material of the second wafer is arranged between the first dielectric material of the second wafer is arranged outside an outer periphery of the second dielectric material of the second wafer; and arranging the second wafer and the first wafer such that the first conductor of the first wafer and the first conductor of the second wafer electrically communicate with each other; wherein the second wafer has a first side and an opposing second side, and the first conductor of the second wafer extends through the second wafer from the first side to the second side, and further comprising: forming a second conductor through the second wafer from the first side to the second side, the second conductor of the second wafer being arranged between the

first dielectric material and the second dielectric material of the second wafer, in the method of Davey, pertaining to claims 13 and 17, according to the teachings of Ahn, with the motivation that, the via structures as taught by Ahn, allow a number of semiconductor wafers to be interconnected in a stacked formation, where the advantage would be to create, for example, a system module that includes a greater amount of integrated circuits while having a much smaller thickness or size.

Allowable Subject Matter

Claim 18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art of record, Davey US Patent 3,663,308 in view of Ahn et al., US Patent 6,395,630, fails to show the following steps of:

Pertaining to claim 18, "the first die assembly including the first conductor of the first wafer, the first dielectric material of the first wafer, the first conductor of the second wafer, the first dielectric material of the second wafer, the first portion of the second dielectric material of the first wafer, and a first portion of the second dielectric material of the second wafer, the second die assembly including the second conductor of the first wafer, the second conductor of the second wafer, a second portion of the second dielectric material of the first wafer, and a second portion of the second dielectric material of the second wafer."

Claims 12, 15, 19, 21-25 and 27-31 are allowed.

The following is an examiner's statement of reasons for allowance:

The closest prior art of record, Davey US Patent 3,663,308 in view of Ahn et al., US Patent 6,395,630, fails to show the following steps of:

Pertaining to independent claim 12, "and at least partially surrounding the second dielectric material with third dielectric material, the third dielectric material being spaced from the second dielectric material."

Pertaining to independent claim 19, "and forming a second outer insulating layer through the first wafer from the first side to the second side and spaced from the first outer insulating layer such that the first outer insulating layer is arranged between the second outer insulating layer and the first conductor insulating layer, the second outer insulating layer being formed of dielectric material."

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

Applicant's arguments, see Remarks, filed 1/3/06, with respect to the rejection(s) of claim(s) 24, 25 and 27-30 under 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Davey US Patent 3,663,308 in view of Ahn et al., US Patent 6,395,630 with respect to claims 13 and 17.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
3/11/06

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